

PATENT COOPERATION TREATY

From Japanese Patent Office
(INTERNATIONAL SEARCH AUTHORITY)

To: HAYASE, Kenichi HAYASE & CO. 13F, NISSAY SHIN-OSAKA Bldg., 3-4-30, Miyahara, Yodogawa-ku, Osaka-shi, Osaka 532-0003 JAPAN	<p style="text-align: center;">PCT</p> <p style="text-align: center;">WRITTEN OPINION OF THE ISA (PCT Rule 43bis)</p>
	Date of Mailing 11 January 2005

Applicant's or agent's file reference P35826-P0	See item 2 below for the subsequent procedure	
International application No. PCT/JP2004/016575	International filing date 09 November 2004	Priority date 11 November 2003
International Patent Classification (IPC) or national classification and IPC Int. Cl ⁷ G11B20/10, 20/14, H03H17/02, 17/06, 21/00		
Applicant Matsushita Electric Industrial Co., Ltd.		

1. This opinion contains indications relating to the following items:

- I ☒ Basis of the opinion
- II ☐ Priority
- III ☐ Non-establishment of report with regard to novelty, inventive step or industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Rule 43.2.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

OMISSION(2 and 3)

Date of completion of this opinion 17 December 2004	
Name and mailing address of the ISA/JP Japanese Patent Office	Authorized officer Telephone No.

I . Basis of the opinion

1. This opinion has been drawn on the basis of the language of international application, unless otherwise indicated below.

OMISSION (2, 3, and 4)

TRANSLATION of related part of Form PCT/ISA/237

WRITTEN OPINION OF THE ISA

International application No. PCT/JP2004/016575
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V Reasoned statement under Rule 43,2.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims	1-10	YES
	Claims	NONE	NO
Inventive Step(IS)	Claims	3-10	YES
	Claims	1, 2	NO
Industrial Applicability (IA)	Claims	1-10	YES
	Claims	NONE	NO

2. CITATIONS AND EXPLANATIONS

Reference 1: JP 2002-269925 A (Matsushita Electric Industrial Co., Ltd.)
2002.09.20

Reference 2: JP 10-214458 A (Matsushita Electric Industrial Co., Ltd.)
1998.08.11

Reference 3: JP 02-260876 A (Toshiba Corporation) 1990.10.23

The invention as defined in Claim 1 has no inventive step in view of References 1 and 2 cited in the International Search Report.

Reference 1 describes the FIR filter that varies a filter coefficient, the equalization error detector 28 that detects an equalization error (which corresponds to the equalizing performance detecting unit), and the correlator 29, the feedback gain adjustor 30 and the filter coefficient update section 31 that update the filter coefficient from the output of the equalization error detector 28 (which corresponds to the equalization coefficient deciding unit) (Paragraphs [0051], [0054]-[0056]).

Reference 2 describes a technique that the PLL circuit 5 extracts a frame sync pulse TMAX from an output of the equalizer circuit (waveform equalizer) 1 (Paragraphs [0007], [0031], [0032]), and it is easy for persons skilled in the art to apply this technique to the technique described in Reference 1.

The invention as defined in Claim 2 has no inventive step in view of References 1 and 2, and Reference 3 cited in the International Search Report.

Reference 3 describes that waveform equalization is not performed after the tap gain of the transversal filter 15 is reset to the initial value before the PLL circuit 24 is synchronized, i.e., locked (page 4, upper right column, lines 9-16, page 4, lower right column, lines 2-10), and it is easy for persons skilled in the art to apply this technique to the techniques described in References 1 and 2.

The inventions as defined in Claims 3 to 10 are not described in any references cited in the International Search Report, nor obvious to persons skilled in the art.